



# PEMD6

50 V, 100 mA NPN/PNP Resistor-Equipped Transistor;  
R1 = 4.7 kΩ, R2 = open

5 January 2023

Product data sheet

## 1. General description

NPN/PNP Resistor-Equipped Transistor (RET) in a ultra small flat lead SOT666 Surface-Mounted Device (SMD) plastic package.

NPN/PNP complement: PEMH7

PNP/PNP complement: PEMB3

## 2. Features and benefits

- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs

## 3. Applications

- Low current peripheral driver
- Controlling IC inputs
- Replaces general-purpose transistors in digital applications

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor; for the PNP transistor with negative polarity</b>						
$V_{CEO}$	collector-emitter voltage	open base	-	-	50	V
$I_O$	output current		-	-	100	mA
R1	bias resistor 1 (input)		3.3	4.7	6.1	kΩ

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	<p style="text-align: center;"><b>SOT666</b></p>	<p style="text-align: center;">006aaa269</p>
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PEMD6	SOT666	plastic, surface-mounted package; 6 leads; 0.5 mm pitch; 1.6 mm x 1.2 mm x 0.55 mm body	<a href="#">SOT666</a>

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PEMD6	D6

## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
<b>Per transistor; for the PNP transistor with negative polarity</b>					
$V_{CBO}$	collector-base voltage	open emitter	-	50	V
$V_{CEO}$	collector-emitter voltage	open base	-	50	V
$V_{EBO}$	emitter-base voltage	open collector	-	5	V
$I_O$	output current		-	100	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$	[1] [2]	200	mW
$T_j$	junction temperature		-	150	°C
$T_{amb}$	ambient temperature		-65	150	°C
$T_{stg}$	storage temperature		-65	150	°C
<b>Per device</b>					
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$	[1] [2]	300	mW

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 μm copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	625	K/W
<b>Per device</b>						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	416	K/W

[1] Device mounted on an FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint.

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor; for the PNP transistor with negative polarity</b>						
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 100 \mu\text{A}$ ; $I_E = 0 \text{ A}$ ; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 2 \text{ mA}$ ; $I_B = 0 \text{ A}$ ; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	50	-	-	V
$I_{CBO}$	collector-base cut-off current	$V_{CB} = 50 \text{ V}$ ; $I_E = 0 \text{ A}$ ; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	100	nA
$I_{CEO}$	collector-emitter cut-off current	$V_{CE} = 30 \text{ V}$ ; $I_B = 0 \text{ A}$ ; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	1	$\mu\text{A}$
		$V_{CE} = 30 \text{ V}$ ; $I_B = 0 \text{ A}$ ; $T_j = 150 \text{ }^\circ\text{C}$	-	-	50	$\mu\text{A}$
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = 5 \text{ V}$ ; $I_C = 0 \text{ A}$ ; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	100	nA
$h_{FE}$	DC current gain	$V_{CE} = 5 \text{ V}$ ; $I_C = 1 \text{ mA}$ ; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	200	-	-	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 5 \text{ mA}$ ; $I_B = 0.25 \text{ mA}$ ; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	-	-	100	mV
R1	bias resistor 1 (input)		3.3	4.7	6.1	kΩ
$C_c$	collector capacitance	$V_{CB} = 10 \text{ V}$ ; $I_E = 0 \text{ A}$ ; $i_e = 0 \text{ A}$ ; $f = 1 \text{ MHz}$ ; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ ; TR1 (NPN)	-	-	2.5	pF
		$V_{CB} = 10 \text{ V}$ ; $I_E = 0 \text{ A}$ ; $i_e = 0 \text{ A}$ ; $f = 1 \text{ MHz}$ ; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ ; TR2 (PNP)	-	-	3	pF

## 11. Test information

### Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

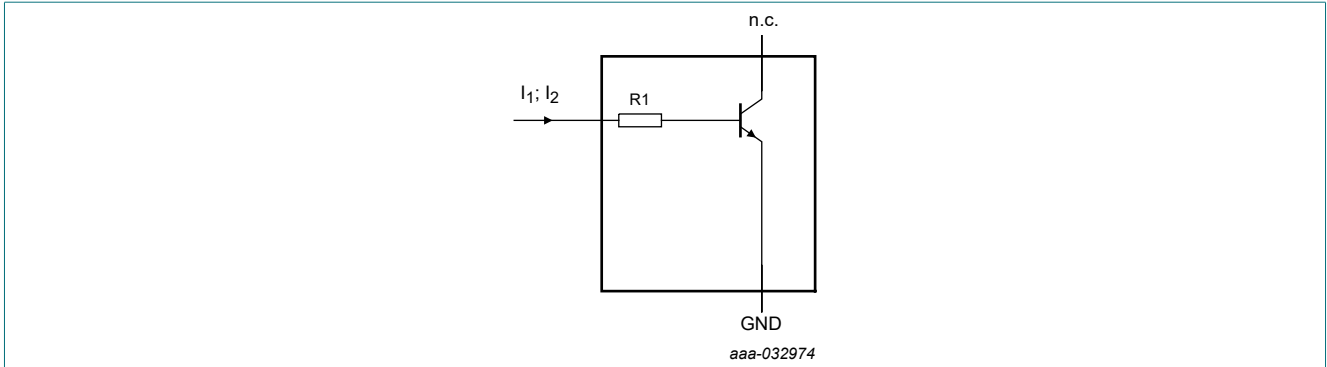


Fig. 1. TR1 (NPN): Resistor test circuit

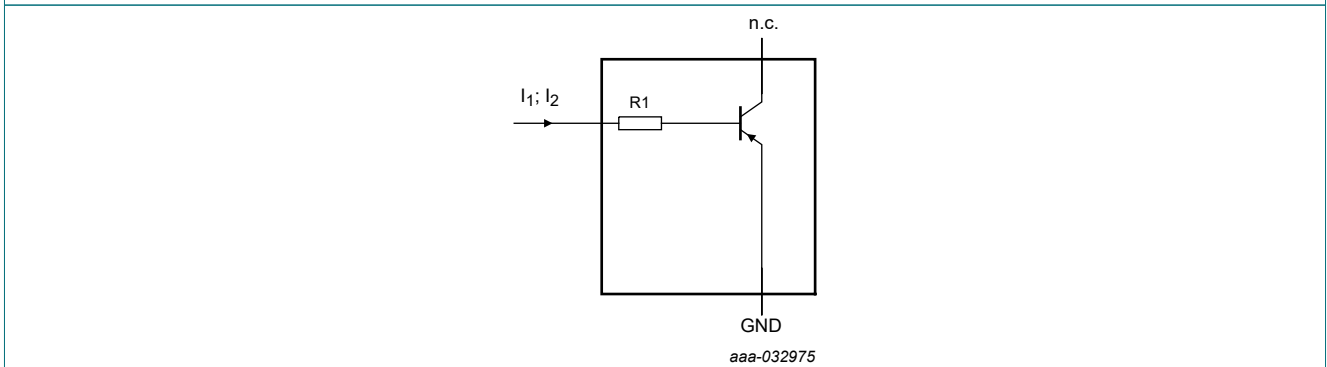


Fig. 2. TR2 (PNP): Resistor test circuit

### Resistor test conditions

Table 8. Resistor test conditions

PEMD6	R1 (kΩ)	R2 (kΩ)	Test conditions	
			I <sub>1</sub>	I <sub>2</sub>
TR1 (NPN)	4.7	open	750 μA	950 μA
TR2 (PNP)	4.7	open	-750 μA	-950 μA

## 12. Package outline

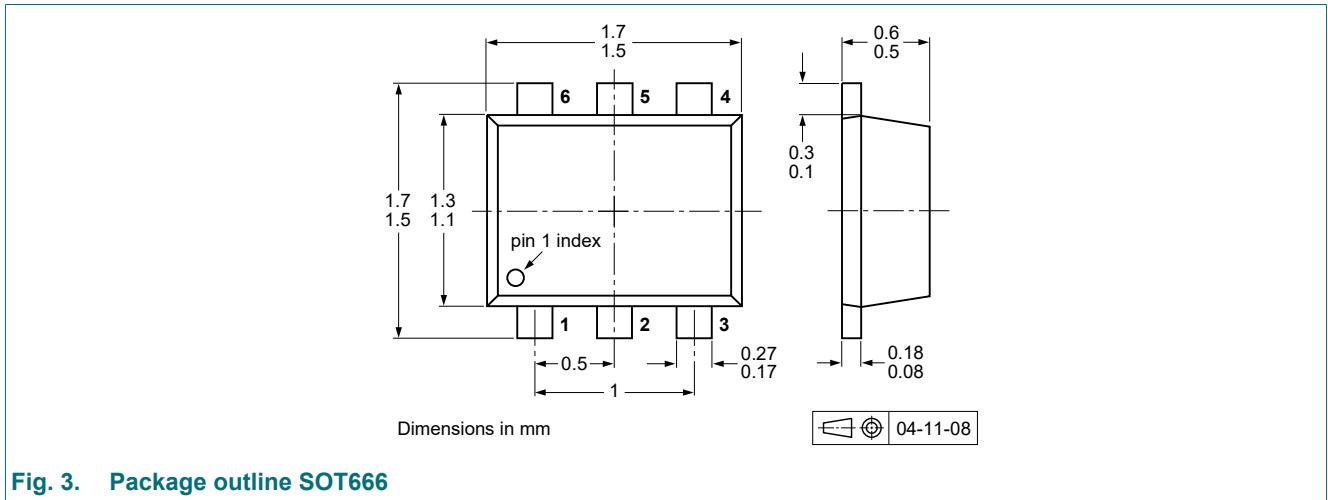


Fig. 3. Package outline SOT666

## 13. Soldering

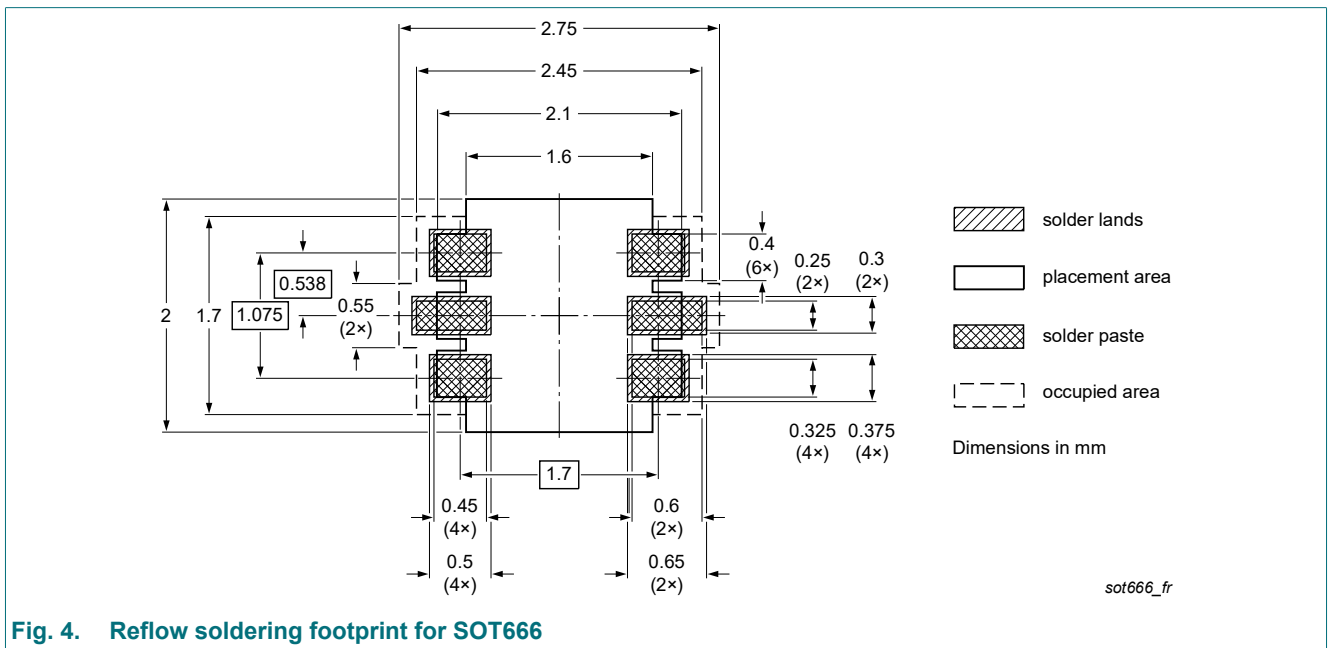


Fig. 4. Reflow soldering footprint for SOT666

## 14. Revision history

**Table 9. Revision history**

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PEMD6 v.4	20230105	Product data sheet	-	PEMD6 v.3
Modifications:	• Section 5 "Pinning Information" table is corrected.			
PEMD6 v.3	20221229	Product data sheet	-	PUMD6_PEMD6 v.2
PUMD6_PEMD6 v.2	20040407	Product data sheet	-	PUMD6_PEMD6 v.1
PUMD6_PEMD6 v.1	20031104	Product specification	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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